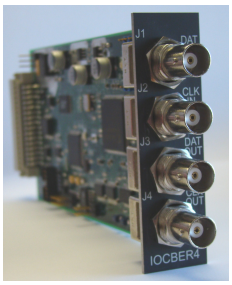
APOGEE LABS

IOCEIM1
ERROR INSERTER MODULE



Sample Picture

FEATURES

- Inserts errors into serial data stream for system evaluation
- Flexible error modes
  - ◊ Grouped, random, and single bit errors
  - ◊ Bit slips, forward, reverse
- Bit rate from 1 Kbps to 35 Mbps NRZ
  - ◊ TTL / LVTTL data and zero degree clock
- Programmable features
  - ◊ Group errors: 0 to 4095 errors every 10^{1} to 10^{10} bits
  - ◊ Random error probability: m x 10^{-n} where m= 1 to 9 and n= 1 to 10
  - ◊ Slip +/- 0 to 15 bits
  - ◊ Input and output clock polarity

OVERVIEW

This combination of the Model AL2873 chassis and Model IOCEIM1 provides a flexible, cost effective means of inserting known errors into a serial data stream. This takes the guess work out of evaluating Error Correcting equipment. It permits processing and display software evaluation under simulated link error conditions, and it allows measurements to be made on certain types of equipment that actually multiply errors (Randomizers and Decryption gear for example).

Up to 14 IOCEIM1 modules may be housed in a single AL2873 chassis. Control of the IOCEIM1 is achieved via the AL2873 chassis front panel or Ethernet remote control.

SPECIFICATIONS

INPUT

- NRZ-L data and 0° or 180° clock
- TTL or LVTTL signal levels
- Jumper selectable termination (50Ω, 75Ω, or 1KΩ)
- BNC type connector
- Rate: 1 Kbps to 35 Mbps

ERROR MODES

- Single Bit Error: Inverts one bit after front panel key depressed or the TTL error insert line on rear panel is toggled
- Grouped Errors, X*10EY where X=1 to 4095 and y=1 to 10: In this mode, the interval (10EY) is derived by simply counting bits. Every time the counter rolls over, the next X bits will be inverted. This provides a very deterministic error insertion mode.
- Random Errors, BER=X*10E-Y where X=1 to 9 and Y=1 to 10: In this mode, several very long, independent PRN generators are decoded to produce the selected error rate. Rather than operate over a fixed interval, every bit time will be subjected to error insertion at the selected error insertion at the selected error probability.
- Bit Slip Delay, n where “n” is the number of bit delays to impose (0 to 16): A 16 bit shift register followed by a 16:1 mux selects the number of bit delays the data is subjected to. This approach avoids deleted, added, or truncated clocks and retains full synchronous operation. Note: whenever the ERROR TYPE is NOT single, the external trigger input will cause the selected Bit Slip Delay to increment by 1, and wrap around from 15 to 0.

OUTPUT

- Signal: TTL level; 0° clock and NRZ-L data; 51Ω / 75Ω driver
- Connectors: TTL BNC; RS-422 Triaxial

REMOTE CONTROL

- Via 10 BaseT Ethernet

ENVIRONMENTAL

- Operating temperature: 0° to 50° C
- Relative humidity: 15% to 95%; non-condensing
- Altitude: Sea level to 10,000 feet

MEAN TIME BETWEEN FAILURES

- ~ 100,000 hours