APOGEE LABS

MODEL 2349

DLTM4
DATA LINK TEST MODULE

FEATURES

- **Independent Transmit & Receive Functions**
- **Bit Rate from 100 bps to 35 Mbps**
  - **Adjustable in 1 bps steps**
- **Internal Synthesizer or External Clock**
  - **20 ppm Accuracy and Stability**
- **Input/Output Bit Code Selection:**
  - **NRZ-L/M/S; BiP-L/M/S;**
  - **RNRZ-L; DM-M/S**
- **Link Delay Measurement**
  - **Round Trip or simplex**
- **Simulates Doppler Shift**
- **User Configurable Measurements**

PURPOSE OF MODULE

The Model 2349 DLTM4 provides the capabilities needed to perform bit-error-rate performance testing of data links and associated hardware, such as PCM bit synchronizers and frame synchronizers. Data bit rates from 100 bps to 35 Mbps are supported. Measurement capabilities include: Bit Error related tests, bit slip tests, and measurement of round trip data link delay.

Basic input and output interfaces included on the module may be supplemented by the addition of I/O interface modules at the system level.

FUNCTIONAL DESCRIPTION

The transmitter and receiver contain independent circuits to generate test data and to receive and detect errors using either pseudo-random number (PRN) data sequences or time division multiplexed (TDM) programmed data values (PCM data). No operator intervention is required to initiate the data synchronization process, regardless of link delays. Data code conversion is included for all IRIG-106 codes. Figure 1 is a functional block diagram of the DLTM4 module.

The PRN Receiver automatically synchronizes a local data generator to the received PRN data sequence. The error free locally generated data stream is compared bit-by-bit to the input data to detect and identify errors.

When using the PCM mode of operation, the format instructions entered into the transmit (TX) memory are copied into the receive (RX) memory. The PCM Receiver monitors the received data stream, locates the frame sync pattern and synchronizes a local data generator to the delayed PCM data being received. Bit by bit comparisons are made between the received data and the local data generator to detect and identify received errors.

The module occupies three slots in an AL4300-LCD or AL6300-LCD chassis.

210 South 3rd Street, North Wales, PA 19454
Tel: 215.699.2060 Fax: 215.699.2061

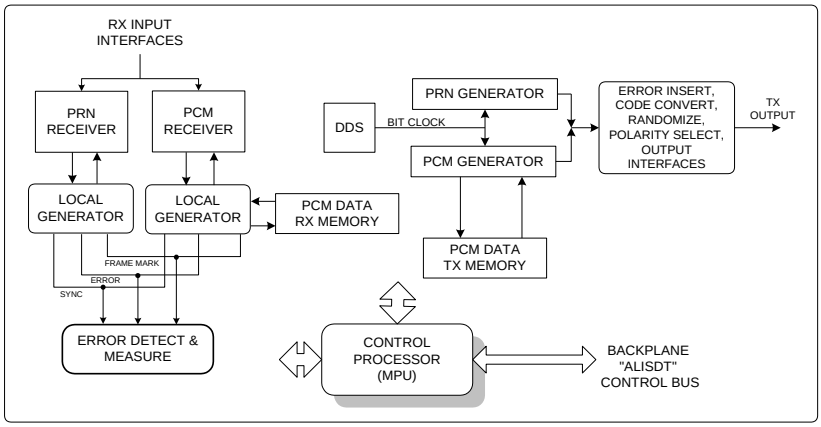

Figure 1: Model 2349 DLTM4 Block Diagram

SPECIFICATIONS

TEST MODES

Accumulate (manual reset and re-start)
Time-Based Interval (1 second to 500 hours)
Bit-Based Intervals (10 to 10^{12} bits)

MEASUREMENTS

Received Bit Rate
Bit Count
Receiver Re-Syncs (slips)
Bit Error Count
Ones in Error
Bit Error Rate
Bit Slip Probability
Symmetry
Frames in Error
Seconds in Test
Seconds in Error
Link Round-Trip Link Delay
One-Way Link Delay

ENVIRONMENT

Operating temperature: 0° to +50° C
Relative Humidity: 0 to 95%, non-condensing
Requires 3 card slots

TX / RX COMMON FEATURES

Bit Codes

NRZ-L/M/S, BIP-L/M/S, DM-M/S, RNRZ-L

PRN Patterns: Forward and Reverse

2^7-1, 2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, 2^{31}-1

TDM Format

4-32 bit Frame Synchronization
Up to 4096 words/frame
8, 16, 32 bits per word
General and Unique Data

TRANSMITTER

Bit Rate

100 bps to 35 Mbps
User selectable Doppler shift rates

Error Injection

One Error per Command
Constant Rate 10^{-2} to 10^{-6} error rates
Uniform or random distribution

Blanking

10 to 4096 bits every 64 to 1024 bits
Free running or Synchronized to frames

Force output to all zeros

Force 1 TX bit slip

RECEIVER

Auto Synchronization

PRN or TDM

Signal Polarity Selection

Clock and/or Data Normal or Inverted

INTERFACES

TTL - 50/75 ohm, BNC Connector
RS422 - 120 ohm
Bipolar Output - 100 bps to 35M bps (2V p-p)

POWER CONSUMPTION

4.8 Watts